

Multimedia Multiprocessor Systems Analysis Design And Management Embedded Systems

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Modern multimedia systems are becoming increasingly multiprocessor and heterogeneous to match the high performance and low power demands placed on them by the large number of applications. The concurrent execution of these applications causes interference and unpredictability in the performance of these systems. In Multimedia Multiprocessor Systems, an analysis mechanism is presented to accurately predict the performance of multiple applications executing concurrently. With high consumer demand the time-to-market has become significantly lower. To cope with the complexity in designing such systems, an automated design-flow is needed that can generate systems from a high-level architectural description such that they are not error-prone and consume less time. Such a design methodology is presented for multiple use-cases -- combinations of active applications. A resource manager is also presented to manage the various resources in the system, and to achieve the goals of performance prediction, admission control and budget enforcement.

This book describes analytical models and estimation methods to enhance performance estimation of pipelined multiprocessor systems-on-chip (MPSoCs). A framework is introduced

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for both design-time and run-time optimizations. For design space exploration, several algorithms are presented to minimize the area footprint of a pipelined MPSoC under a latency or a throughput constraint. A novel adaptive pipelined MPSoC architecture is described, where idle processors are transitioned into low-power states at run-time to reduce energy consumption. Multi-mode pipelined MPSoCs are introduced, where multiple pipelined MPSoCs optimized separately are merged into a single pipelined MPSoC, enabling further reduction of the area footprint by sharing the processors and communication buffers. Readers will benefit from the authors' combined use of analytical models, estimation methods and exploration algorithms and will be enabled to explore billions of design points in a few minutes.

This book describes a new, coarse-grained reconfigurable architecture (CGRA), called Blocks, and puts it in the context of computer architectures, and in particular of other CGRAs. The book starts with an extensive evaluation of historic and existing CGRAs and their strengths and weaknesses. This also leads to a better understanding and new definition of what distinguishes CGRAs from other architectural approaches. The authors introduce Blocks as unique due to its separate programmable control and data paths, allowing light-weight instruction decode units to be arbitrarily connected to one or more functional units (FUs) over a statically configured interconnect. The discussion includes an explanation of how to model architectures, resulting in an area and energy model for Blocks. The accuracy of this model is evaluated against fully implemented architectures, showing that although it is three orders of magnitude faster than synthesis the error margin is very acceptable. The book concludes with a case study on a real System-on-Chip, including a RISC architecture, the Blocks CGRA and peripherals.

This book discusses analysis, design and optimization techniques for streaming multiprocessor systems, while satisfying a given area, performance, and energy budget. The authors describe design flows for both application-specific and general purpose streaming systems. Coverage also includes the use of machine learning for thermal optimization at run-time, when an application is being executed. The design flow described in this book extends to thermal and energy optimization with multiple applications running sequentially and concurrently.

The first book to survey this emerging field in digital system design.

Techniques for Optimizing Multiprocessor Implementations of Signal Processing Applications
An indispensable component of the information age, signal processing is embedded in a variety of consumer devices, including cell phones and digital television, as well as in communication infrastructure, such as media servers and cellular base stations. Multiple programmable processors, along with custom hardware running in parallel, are needed to achieve the computation throughput required of such applications. Reviews important research in key areas related to the multiprocessor implementation of multimedia systems
Embedded Multiprocessors: Scheduling and Synchronization, Second Edition presents architectures and design methodologies for parallel systems in embedded digital signal processing (DSP) applications. It discusses application modeling techniques for multimedia systems, the incorporation of interprocessor communication costs into multiprocessor scheduling decisions, and a modeling methodology (the synchronization graph) for multiprocessor system performance analysis. The book also applies the synchronization graph model to develop hardware and software optimizations that can significantly reduce the interprocessor communication overhead of a given schedule. Chronicles recent activity

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dealing with single-chip multiprocessors and dataflow models This edition updates the background material on existing embedded multiprocessors, including single-chip multiprocessors. It also summarizes the new research on dataflow models for signal processing that has been carried out since the publication of the first edition. Harness the power of multiprocessors This book explores the optimization of interprocessor communication and synchronization in embedded multiprocessor systems. It shows you how to design multiprocessor computer systems that are streamlined for multimedia applications.

This book gives a comprehensive introduction to the design challenges of MPSoC platforms, focusing on early design space exploration. It defines an iterative methodology to increase the abstraction level so that evaluation of design decisions can be performed earlier in the design process. These techniques enable exploration on the system level before undertaking time- and cost-intensive development.

Dynamic and Robust Streaming in and between Connected Consumer-Electronic Devices addresses a subject that is becoming more important over the years. On the one hand the arrival of home networks is imminent, and on the other hand we notice that chips integrate more and more functionality. The home network interconnects the Consumer Electronic (CE) devices in the home, and the individual CE-devices incorporate the chips to realize a ubiquitous streaming of video streams over this network. This book provides a comprehensive overview of the challenges that face us. The book shows that there are many similarities between traditional networking and networks in the chip. However, there are some different operational conditions that lead to original solutions. Dynamic and Robust Streaming in and between Connected Consumer-Electronic Devices focuses on the robustness aspects of the chosen technologies in the area of video streaming. Management of resources such as memory, bandwidth, CPU cycles, bus-cycles is an aspect that is prominent in many of the sections.

The SAMOS workshop is an international gathering of highly qualified researchers from academia and industry, sharing in a 3-day lively discussion on the quiet and - spiring northern mountainside of the Mediterranean island of Samos. As a tradition, the workshop features workshop presentations in the morning, while after lunch all kinds of informal discussions and nut-cracking gatherings take place. The workshop is unique in the sense that not only solved research problems are presented and discussed but also (partly) unsolved problems and in-depth topical reviews can be unleashed in the scientific arena. Consequently, the workshop provides the participants with an environment where collaboration rather than competition is fostered. The earlier workshops, SAMOS I–IV (2001–2004), were composed only of invited presentations. Due to increasing expressions of interest in the workshop, the Program Committee of SAMOS V decided to open the workshop for all submissions. As a result the SAMOS workshop gained an immediate popularity; a total of 114 submitted papers were received for evaluation. The papers came from 24 countries and regions: Austria (1), Belgium (2), Brazil (5), Canada (4), China (12), Cyprus (2), Czech Republic (1), Finland (15), France (6), Germany (8), Greece (5), Hong Kong (2), India (2), Iran (1), Korea (24), The Netherlands (7), Pakistan (1), Poland (2), Spain (2), Sweden (2), Taiwan (1), Turkey (2), UK (2), and USA (5). We are grateful to all of the authors who submitted papers to the workshop.

This book serves as a reference for researchers and designers in Embedded Systems who need to explore design alternatives. It provides a design space exploration methodology for the analysis of system characteristics and the selection of the most appropriate architectural solution to satisfy requirements in terms of performance, power consumption, number of

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required resources, etc. Coverage focuses on the design of complex multimedia applications, where the choice of the optimal design alternative in terms of application/architecture pair is too complex to be pursued through a full search comparison, especially because of the multi-objective nature of the designer ' s goal, the simulation time required and the number of parameters of the multi-core architecture to be optimized concurrently.

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